an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region[.] ; and

the memory device further comprises:

a row decoder;

a column decoder;

a command and control circuit;

a voltage control circuit; and

wherein the memory cells are arranged in an array.

68. (Amended) The memory device of claim 67 wherein:

the floating gate comprises polycrystalline or microcrystalline silicon carbide;

a barrier energy between the floating gate and the insulator is less than approximately 3.3 eV;

the insulator comprises a material that has a larger electron affinity than silicon dioxide;

an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region[.] ; and

the memory device further comprises:

a row decoder;

a column decoder;

a command and control circuit;

a voltage control circuit; and

wherein the memory cells are arranged in an array.

70. (Amended) The memory device of claim 69 wherein:

a barrier energy between the floating gate and the insulator is less than approximately 3.3 eV;

the floating gate comprises a material that has a smaller electron affinity than polycrystalline silicon; [and]

the insulator comprises a material that has a larger electron affinity than silicon dioxide[.]; and

the memory device further comprises:

a row decoder;

a column decoder;

a command and control circuit;

a voltage control circuit; and

wherein the memory cells are arranged in an array.

Please add the following new claims:

73. (New) A memory cell comprising:

a storage electrode to store charge, the storage electrode comprising a material that has a smaller electron affinity than polycrystalline silicon;

an insulator adjacent to the storage electrode, wherein a barrier energy between the insulator and the storage electrode is less than approximately 3.3 eV; and

a control electrode, separated from the storage electrode by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide.

74. (New) The memory cell of claim 73, further comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region; and

wherein the insulator is between the storage electrode and the channel region, the insulator comprising a material that has a larger electron affinity than silicon dioxide; and

wherein an area of a capacitor formed by the control electrode, the storage electrode, and the intergate dielectric is larger than an area of a capacitor formed by the storage electrode, the insulator, and the channel region.

75. (New) A memory device comprising:

a plurality of memory cells, wherein each memory cell includes a transistor comprising:

a source region;

a drain region;

a channel region between the source and drain regions;

a floating gate separated from the channel region by an insulator, the floating gate comprising a material that has a smaller electron affinity than polycrystalline silicon and a barrier energy between the floating gate and the insulator being less than approximately 3.3 eV; and

a control gate separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide.

76. (New) The memory device of claim 75 wherein:

the floating gate comprises polycrystalline or microcrystalline silicon carbide;

the insulator comprises a material that has a larger electron affinity than silicon dioxide;

an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region; and

the memory device further comprises:

a row decoder;

a column decoder;

a command and control circuit;

a voltage control circuit; and

wherein the memory cells are arranged in an array.

77. (New) A memory device comprising:

a plurality of memory cells, wherein each memory cell includes a transistor comprising:

a source region;

a drain region;

a channel region between the source and drain regions;

a floating gate separated from the channel region by an insulator, the floating gate being capacitively separated from the channel region to provide transconductance gain; and

a control gate separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide.

78. (New) The memory device of claim 77 wherein:

the floating gate comprises polycrystalline or microcrystalline silicon carbide and has a smaller electron affinity than polycrystalline silicon;

a barrier energy between the floating gate and the insulator is less than approximately 3.3 eV;

the insulator comprises a material that has a larger electron affinity than silicon dioxide;

an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region; and

the memory device further comprises:

a row decoder;

a column decoder;

a command and control circuit;

a voltage control circuit; and

wherein the memory cells are arranged in an array.